



Binary Neural-Networks for FPGAs

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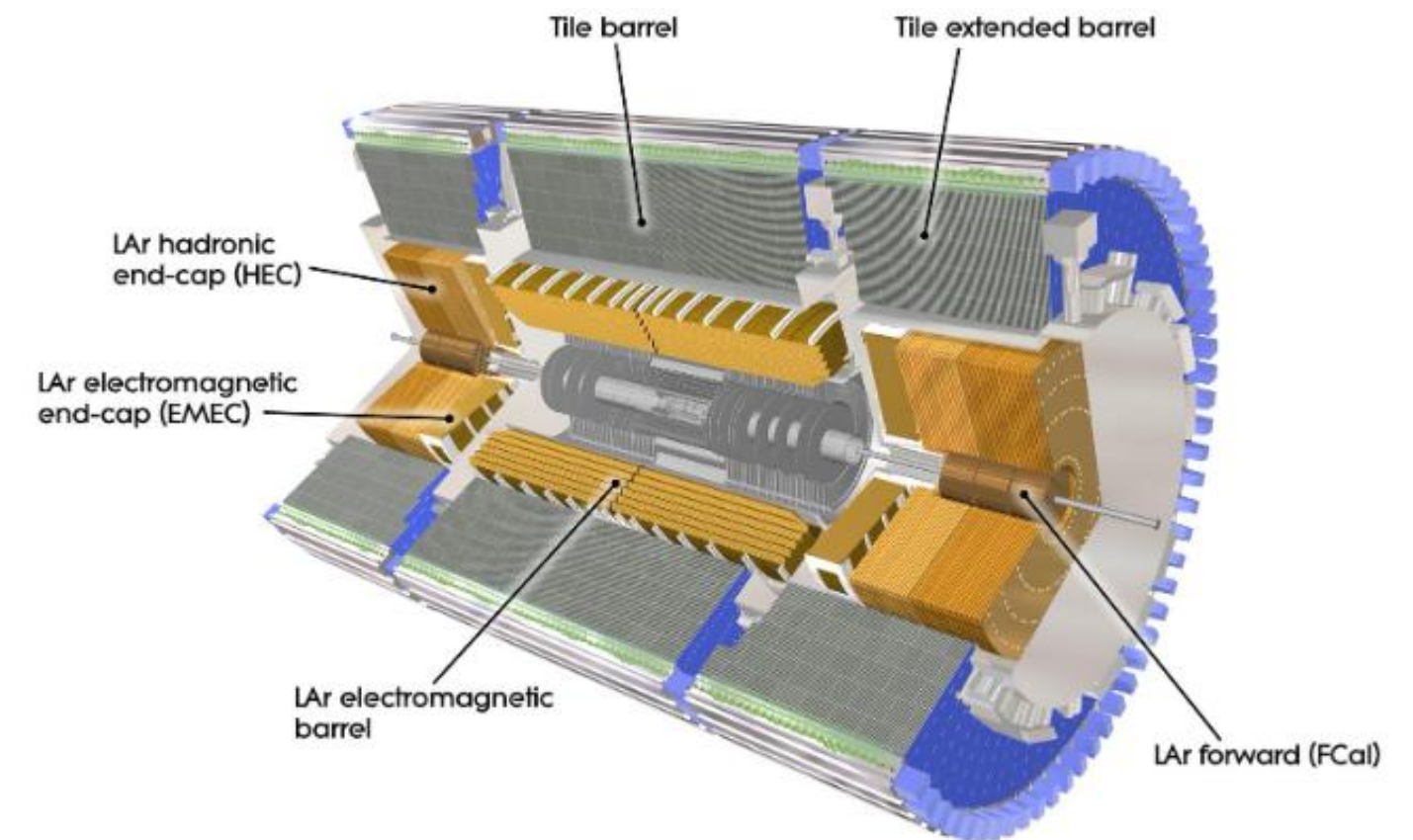
Binary Neural-Networks for FPGAs

Part of the **ATLAS** Phase-II Upgrade, within the **Next Generation Global Trigger** project

Data from the **Liquid Argon (LAr)** electromagnetic **calorimeter** for real-time **tau** particles identification at the Level-1 hardware trigger

Field Programmable Gate Arrays (FPGAs) - reprogrammable chips for low-latency, parallel processing in trigger systems

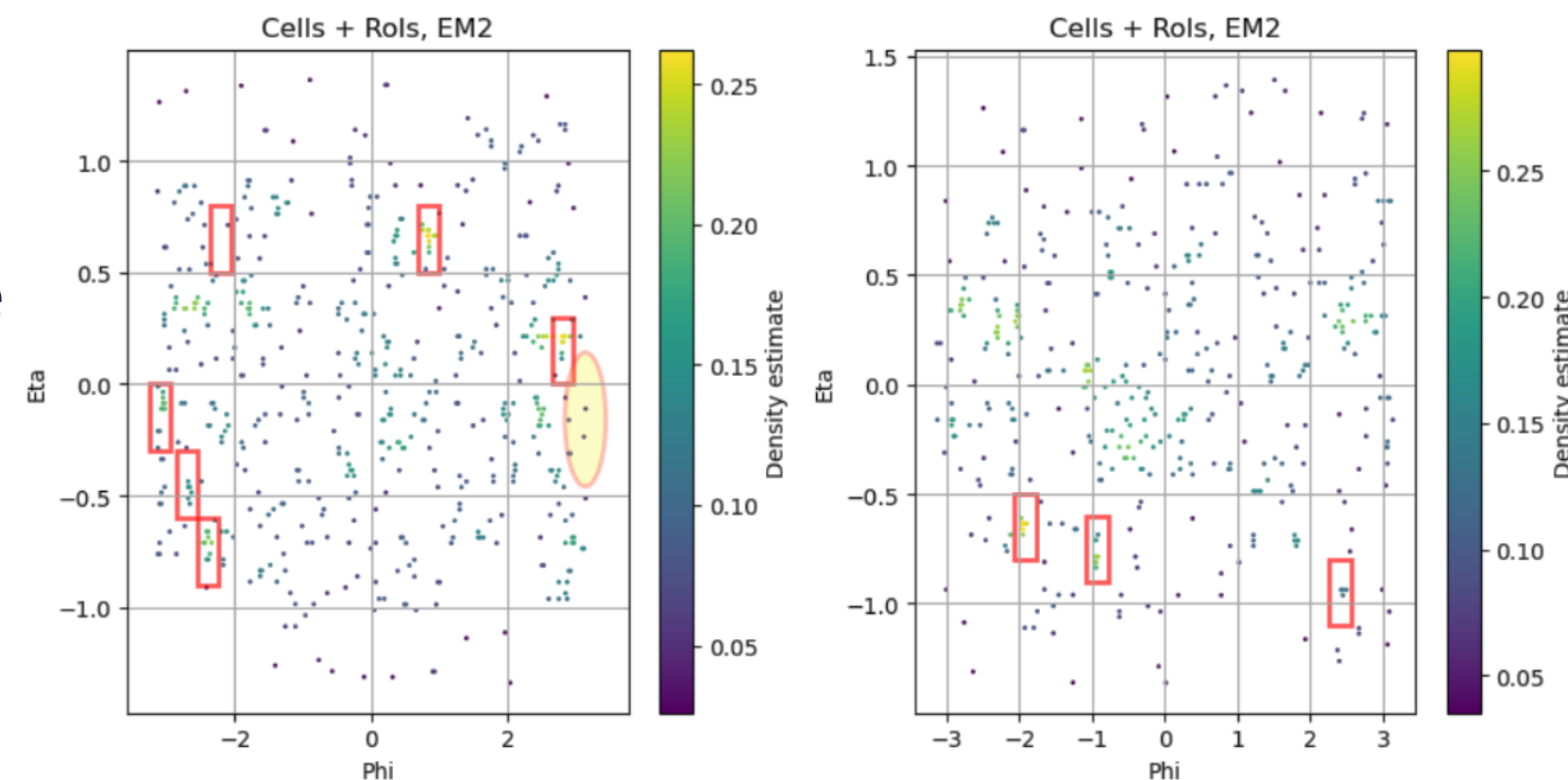
Binary Neural Networks (BNNs) - neural networks with binary weights & activations, reducing resource and power consumption for efficient FPGA implementation



Project Overview

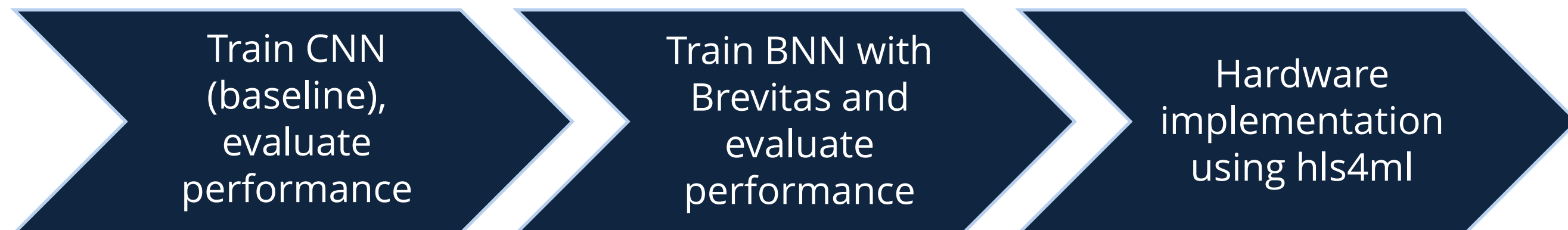
Input Data

- Each event is a 12×12 image of energy deposits from the Liquid Argon electromagnetic calorimeter.
- Images are centered on Level-1 trigger tau seeds (provided by the first stage calorimeter processing).
- **Signal:** Events with tau decays from a $\gamma^* \rightarrow \tau\tau$ sample, matched to the truth information.
- **Background:** Events from a low-pT jet sample (0–20 GeV) containing tau seeds from jets.



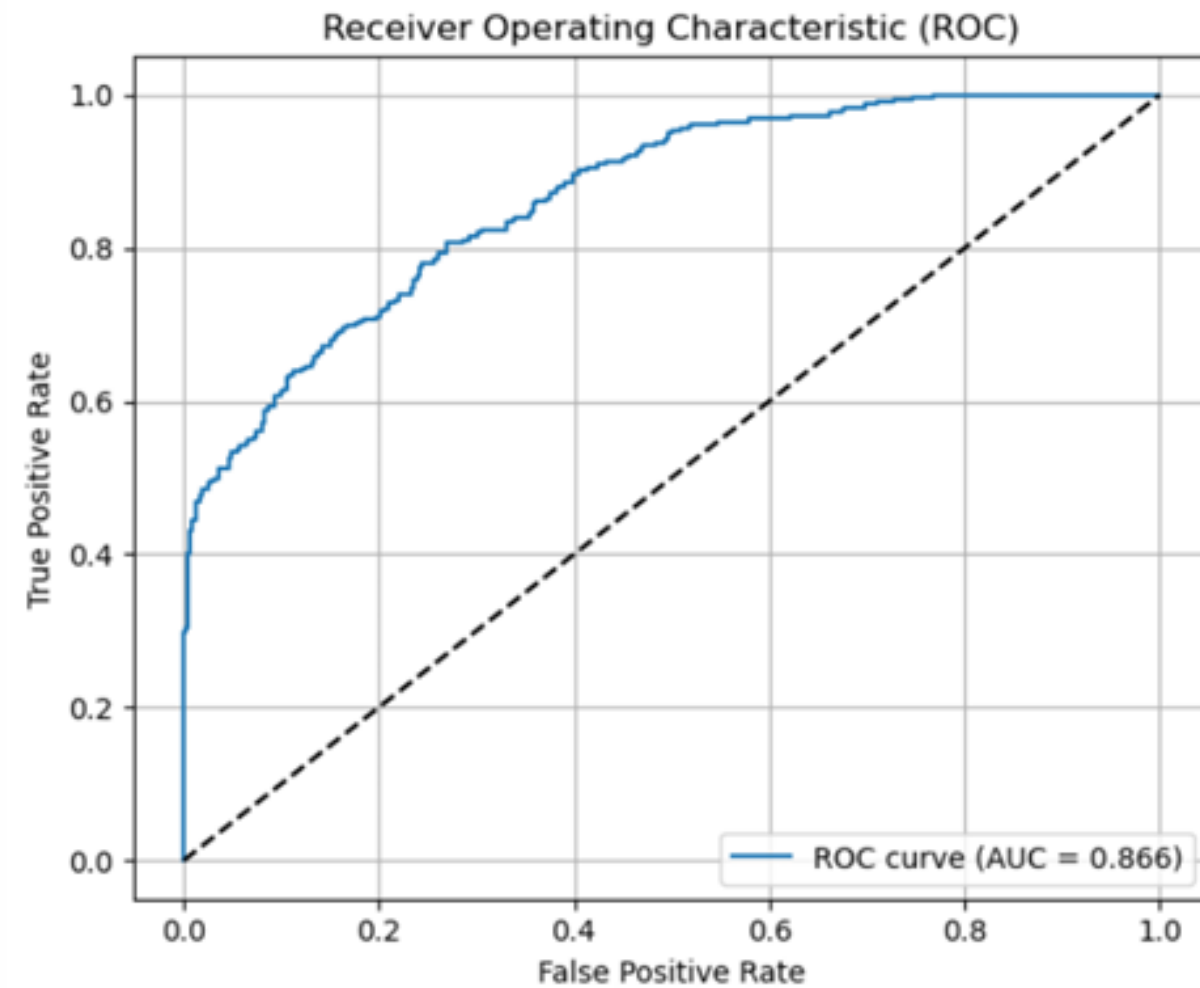
Goal: Train and compare two models. A full-precision CNN and a Binary Neural Network to classify tau candidates vs jets, and prepare the BNN for FPGA implementation.

Workflow

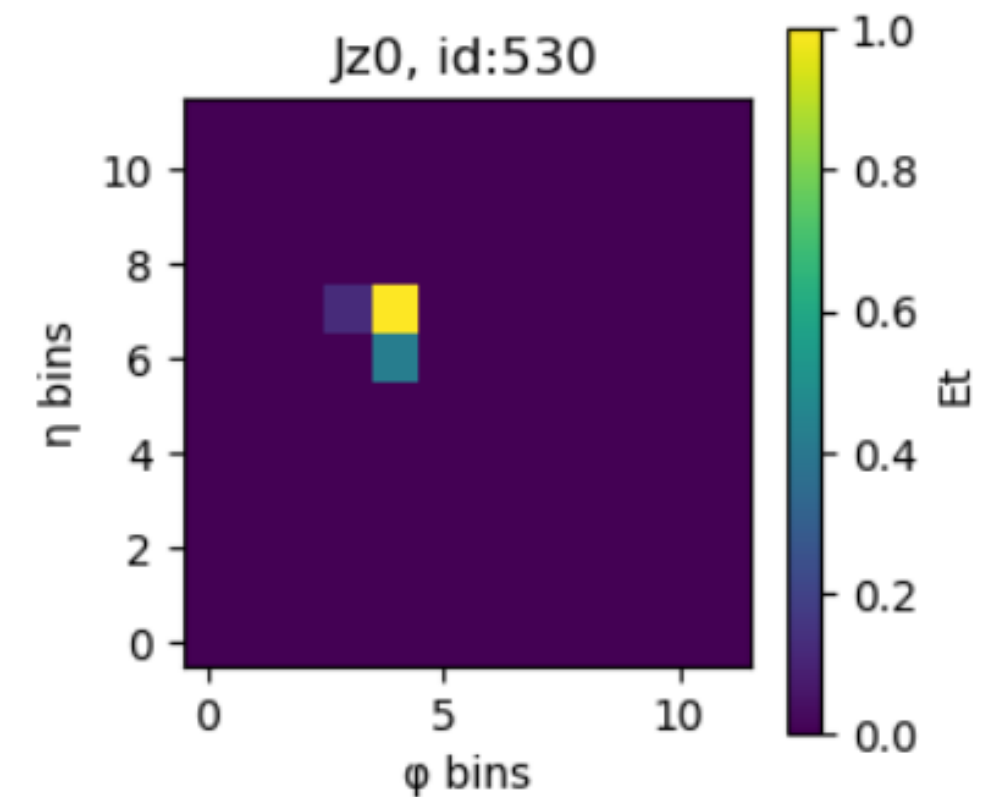
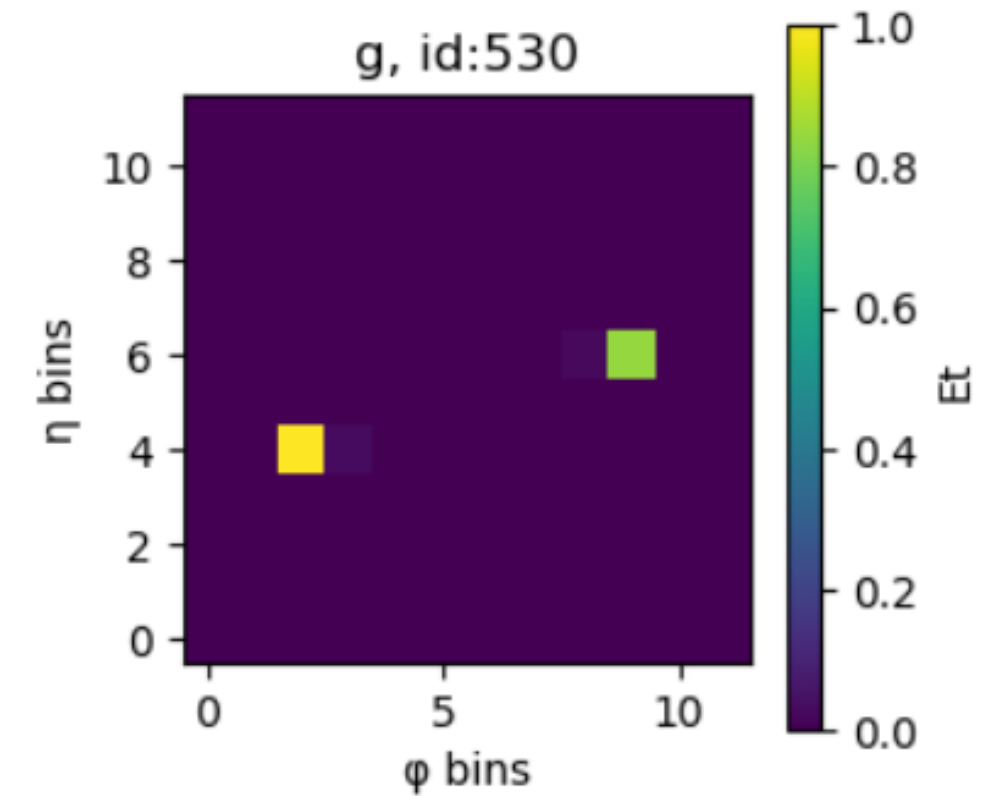


CNN Baseline

- Built baseline CNN architecture for classification
- Evaluated with ROC curve (AUC = 0.886).
- Area Under Curve summarizes the classifier's performance between signal efficiency and background rejection
- Serves as reference model for BNN comparison.

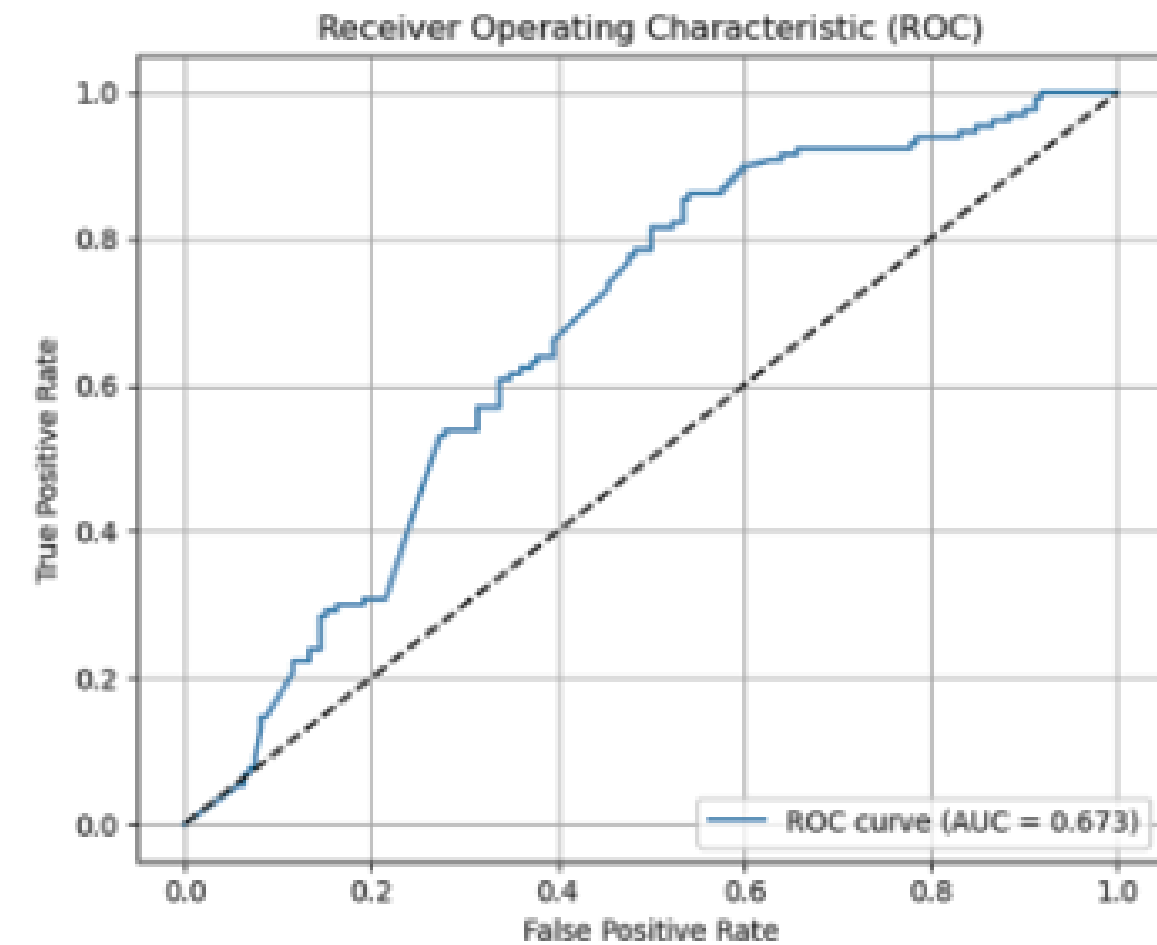
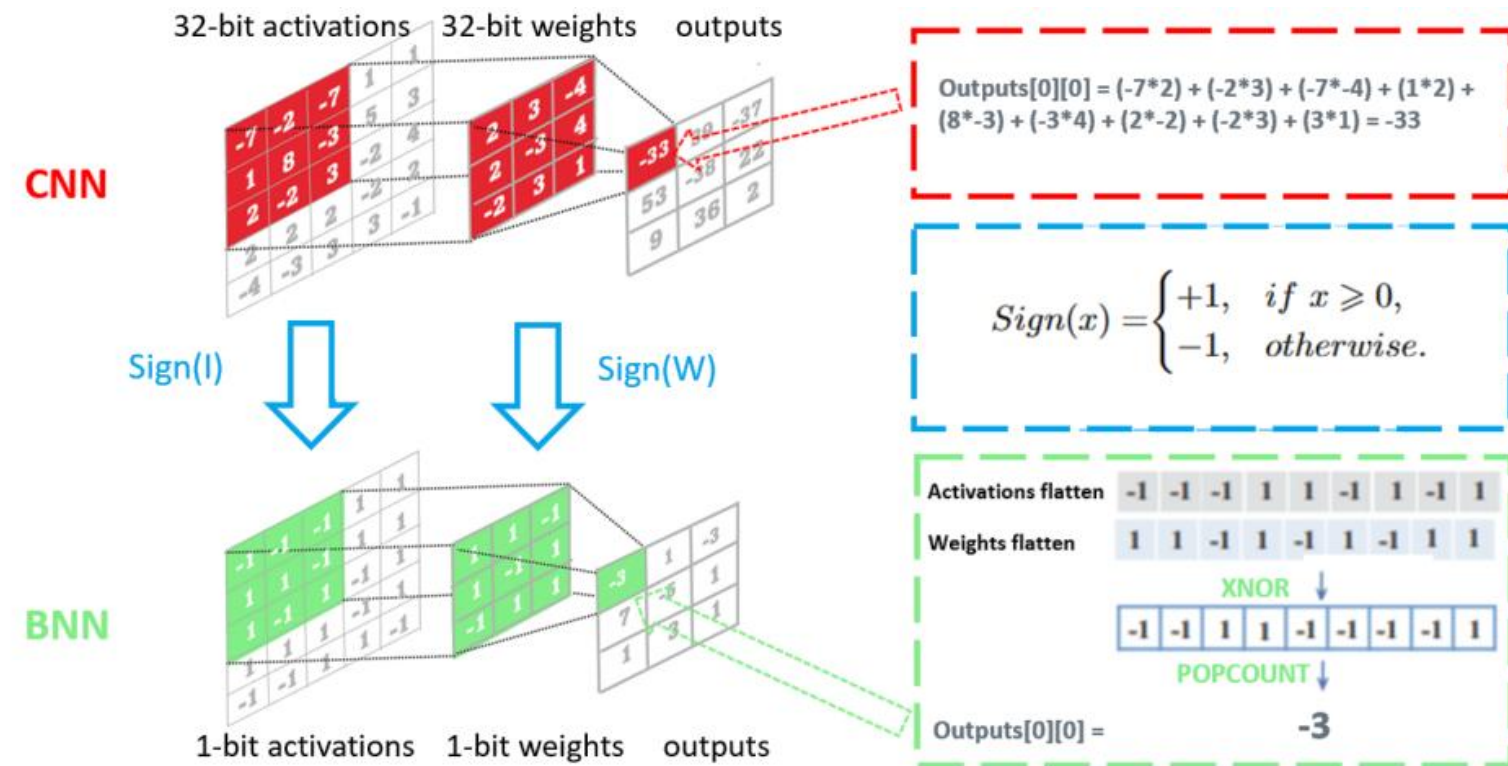


ROC AUC: 0.8661



BNN

- Implemented with **Brevitas** (PyTorch quantization library)
- Based on Bi-Real Net architecture → shortcuts for gradient stability
- 32-bit activations & weights in the CNN → 1-bit (± 1) in convolutions
- Performance of first results, AUC (~ 0.67), lower accuracy



Summary

- CNN baseline achieves good classification for tau seed identification (AUC ~ 0.89)
- First BNNs show lower accuracy for the first results due to reducing precision from 32-bit to 1-bit weights and activations.
- Confirms feasibility of using BNNs for FPGA deployment.

Next Steps

- Optimize CNN & BNN architectures
- Implement BNNs in hls4ml for FPGA synthesis
- Measure hardware metrics (latency, resource usage, power)

Thank you!

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